REMARKS

Applicant respectfully requests reconsideration and allowance of the subject application. Claim 22 has been amended. Claims 7-13 and 19-33 are pending.

35 U.S.C. §112

Claim 22 is rejected under 35 U.S.C. §112, second paragraph, as being indefinite. Claim 22 has been amended to recite "wherein the active areas are electrically isolated by the deposited layer of oxide". Accordingly, withdrawal of the rejection is respectfully requested.

35 U.S.C. §102

Claims 24 and 26-31 are rejected under 35 U.S.C. §102(e) as being anticipated by U.S. Patent No. 6,200,862 to Gardner et al. (hereinafter, "Gardner"). The Applicant respectfully traverses the rejection.

Claim 24 recites a method that includes "depositing a layer of oxide proximate a first surface of a semiconductor substrate", "exposing a portion of the first surface of the semiconductor substrate", and "forming a pair of active areas in the exposed portion of the first surface, adjacent the deposited oxide layer". Gardiner does not disclose, teach or suggest these aspects.

As previously discussed, Gardner discloses that "[S]ubstrate 10 has already had formed therein, e.g., by ion implantation, a channel region 14, a punch-through region, and a well region." (*emphasis added.*) *Gardner, Col. 3, Lines 24-31.* Gardner then discloses that "[a]fter formation of doped regions in the substrate 10, a gate dielectric layer 22, of 10-30 ANG. is formed by oxide growth, plasma deposition, or low pressure chemical vapor deposition." *Gardner, Col 3, Lines 52-55.* After which, Gardner discloses a patterning of

layer 30 for ion bombardment to form a resulting device having asymmetric source/drain regions. *See Gardner, Col. 4, Lines 14-36.* Thus, Gardner only discloses the formation of the dielectric layer 40 after the formation of the source/drain regions.

Nowhere in Gardner is there discussion, teaching or suggestion "depositing a layer of oxide," "exposing a portion of the first surface of the semiconductor substrate", and then "forming a pair of active areas **in the exposed portion of the first surface**" as recited in claim 24. (emphasis added).

Further, assertions made by the Office support that Gardner does not teach or disclose "exposing a portion of the first surface of the semiconductor substrate", and then "forming a pair of active areas in the exposed portion of the first surface" as recited in claim 24. For example, as correctly asserted by the Examiner at page seven of the *Office Action Dated March 31, 2004,* "Gardner et al. teach forming the deposited oxide layer 40 *after* forming the active areas 28/24". The Examiner also correctly states at page 5 in the *Office Action Date July 15, 2004* that "Garner et al. do not teach forming the pair of active areas 28/34 after depositing the layer oxide". For at least these reasons, claim 24 is allowable over Gardner. Applicant respectfully requests that the §102 rejection of claim 24 be withdrawn.

Claims 26-31 depend from claim 24 and are allowable for at least the same reasons as stated with respect to claim 24. These claims are also allowable for their own recited features, which are not disclosed, taught or suggest by the submitted references, alone or in combination. Accordingly, Applicant respectfully requests that the §102 rejection of claims 26-31 be withdrawn.

35 U.S.C. §103

Claims 7, 9-13 and 32 are rejected under 35 U.S.C. §103(a) as being unpatentable over Gardner in view of U.S. Patent No. 5,635,968 to Bhaskar et al. (hereinafter, "Bhaskar"). The Applicant respectfully traverses the rejection.

Claim 7 recites a method that includes "depositing a layer of oxide proximate a first surface of a semiconductor substrate" and "***after the depositing of the layer of oxide,*** forming a pair of active areas in the first surface, adjacent the deposited oxide layer and gate oxide layer". (emphasis added). Neither Gardner nor Bhaskar, alone or in combination, disclose, teach or suggest these aspects.

As previously described, Gardiner does not disclose, teach or suggest "***after the depositing of the layer of oxide,*** forming a pair of active areas in the first surface, adjacent the deposited oxide layer and gate oxide layer". (emphasis added). As previously described, this statement is also supported by the Office. For example, as correctly stated at page seven in the *Office Action Dated March 31, 2004,* "Gardner et al. teach forming the deposited oxide layer 40 *after* forming the active areas 28/24". The *Office Action Dated July 15, 2004* also correctly asserts at page 5 that "Garner et al. do not teach forming the pair of active areas 28/34 after depositing the layer oxide".

The Examiner then asserts Bhaskar to correct the defects of Gardiner, stating that "Bhaskar et al., in an analogous art, teach forming the oxide layer 903 by CVD (Fig. 9); forming an opening in the oxide layer 903 and then forming the active areas 907 and 911". The Applicant respectfully disagrees. Bhaskar does not disclose, teach or suggest an order in which the components of the Bhaskar device are formed, as shown in the following excerpt:

> FIG. 9 illustrates a portion of the multi-layer substrate 103 which, in a preferred embodiment, has a lower portion 901 manufactured of P-type monocrystalline silicon and

> preferably has a thickness of about 24-26 mils. The substrate 103 further includes an upper layer 903 of silicon dioxide which is formed by thermal oxidation. Alternatively, upper layer 903 may be formed by a CVD process, heating the lower portion 901 in a mixture of silane, oxygen, and argon at a temperature of about 300-400 degrees C. until the desired thickness of silicon dioxide has been formed, as discussed in U.S. Pat. No. 4,513,298. Another alternative is the use of an upper layer 903 which comprises a combination of a thermally grown oxide layer and a CVD layer as described above (but not shown). In any event the upper layer 903 has a preferred thickness of about 10,000-24,000 angstroms.
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> Integrally formed on the substrate 103 is a plurality of drive transistors, one of which is schematically illustrated at reference number 905 in FIG. 9. Basically, the transistor 905 is of the field effect silicon-gate variety, and includes a source diffusion 907, gate 909, and drain diffusion 911, all of which define electrical contact regions to which various components (e.g. resistors) and electrical circuitry may be connected. *See Bhaskar, Col. 10, Lines 28-50.*

As clarified by the above excerpt, Bhaskar merely describes a substrate that includes an upper layer of silicon dioxide and a plurality of drive transistors formed on the substrate and is completely silent as to the order, sequence, or timing of formation upper layer 903 and transistor 905. Therefore, Bhaskar, alone or in combination with the other submitted references, does not disclose, teach or suggest an order in which the silicon dioxide and drive transistors are formed. This is also supported by the assertions made by the Examiner. For example, as correctly asserted at page 4 in the *Office Action Dated March 31, 2004* in relation to Claim 22, "Bhaskar et al. are silent as to the associated active areas 907 and 911 are formed after the exposing in the first surface of the semiconductor substrate 901". Accordingly, for at least these reasons, claim 7 is allowable over Gardner in view of Bhaskar and withdrawal of the rejection is respectfully requested.

Claims 9-13 and **32** depend from claim 7 and are allowable for at least the same reasons as stated with respect to claim 7. These claims are also allowable for their own recited features, which are not disclosed, taught or suggest by the submitted references, alone or in combination. Accordingly, Applicant respectfully requests that the §103 rejection of claims 9-13, and 32 be withdrawn.

Claim 8 is rejected under 35 U.S.C. §103(a) as being unpatentable over Gardner in view of Bhaskar, and further in view of U.S. Published Patent Application Number 2003/0081070 to Liu et al (hereinafter "Liu"). The Applicant respectfully traverses the rejection.

Claim 8 is a dependent claim which depends from independent claim 7 and is therefore allowable for at least the same reason as claim 7. Further, neither Gardner, Bhaskar, nor Liu, alone or in combination, disclose teach or suggest "thermally growing a thermal oxide layer", after which "depositing a layer of oxide" is performed, and "after the depositing of the layer of oxide, forming a pair of active areas". Accordingly, for at least this reason, claim 8 is allowable over Gardner, Bhaskar and Liu.

Claims 22-23 are rejected under 35 U.S.C. §103 as being unpatentable over U.S. Patent No. 5,635,968 to Bhaskar et al. (hereinafter, "Bhaskar") in view of U.S. Published Application No. 2002/0058368 to Tseng (hereinafter, "Tseng"). Applicant respectfully traverses the rejection.

Claim 22 has been amended to correct informalities and, as amended, recites a method [portions of the amended language appear in bold italics below] comprising:

- depositing a layer of oxide proximate a first surface of a semiconductor substrate;
- exposing a portion of the first surface of the semiconductor substrate; and

- forming a field effect transistor (FET) on the exposed portion of the first surface of the substrate having the deposited oxide layer, wherein the FET includes a gate electrode with associated active areas formed after the exposing the first surface of the semiconductor substrate, and ***wherein the active areas are*** electrically isolated by the deposited layer of oxide.

Support for this amendment can be found throughout the application as originally filed. Neither Bhaskar nor Tseng, alone or in combination, disclose or suggest these aspects.

The Office Action asserts Bhaskar for teaching a method of forming a semiconductor device. The Office Action then asserts Tseng for "forming a deposited oxide 48 on the substrate 42 (Fig. 2A); exposing a first surface (i.e. top surface) of the substrate 42 via a formation of a trench 51 (Fig. 2B); and forming active area 52 (i.e. impurity region by ion implanting through the trench 51 after exposing the first surface (Fig. 2B)." *Office Action Dated March 31, 2004, Page 5.* Tseng, however, describes removal of the sacrificial layer 48, as shown in the following excerpts:

> First, a sacrificial layer 48 and a first photoresist layer 50 are sequentially formed on the substrate 42. The sacrificial layer 48 is formed by depositing a pad oxide layer and a silicon nitride layer on the substrate 42. The photoresist layer 50 is patterned to expose a first predetermined area of the sacrificial layer 48 on region B. As shown in FIG. 2B, by using the first photoresist layer 50 as a mask, a first trench 51 is formed in the sacrificial layer 48 to expose the substrate 42, and then the first photoresist layer 50 is stripped off. Next, using the sacrificial layer 48 as a mask, n-type impurity ions are implanted into the exposed substrate 12 to form a first impurity layer 52. *Tseng, Paragraph 20, Lines 10-21.*
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> As shown in FIG. 2E, a gate insulating layer 56 is formed on the bottom of the first trench 51, the second trench 53, and the third trench 53, and a polysilicon layer 58 is then deposited on the substrate 42 to fill the first trench 51, the

> second trench 53, and the third trench 53. Next, by using a mask, the polysilicon layer 58 and ***the sacrificial layer 48 outside the trenches 51, 53, 55 are removed***. As a result, as shown in FIG. 2F, the polysilicon layer 58 remaining in the second trench 53 on region A serves as a gate electrode 58a of the internal circuit device, the polysilicon layer 58 remaining in the third trench 55 on region B serves as a gate electrode 58b of the ESD protecting device, and the polysilicon layer 58 remaining in the first trench 51 over the first impurity layer 52 on region B serves as a dummy gate electrode 58c of the internal circuit device. *Tseng, Paragraph 22 (emphasis added).*

Thus, Tseng describes that "by using a mask, the polysilicon layer and the sacrificial layer 48 outside the trenches 15, 53, 55 are removed." *Tseng, Paragraph 22, Lines 5-6.* Because Tseng describes the removal of the sacrificial layer 48, as a consequence, the sacrificial layer 48 is not included in the FET described by Tseng and the sacrificial layer 48 does not electrically isolate the associated active areas of the FET. Nowhere in Bhaskar nor Tseng, alone or in combination, is there discussion, teaching or suggestion for the depositing, exposing and forming as claimed in claim 22. Accordingly, for at least this reason, claim 22 is allowable over Bhaskar and Tseng.

Claim 23 depends from claim 22 and is allowable for at least the same reasons as stated with respect to claim 22. Therefore, Applicant respectfully requests that the §103 rejection of claim 23 be withdrawn.

Claims 19-21 and 33 are rejected under 35 U.S.C. §103 as being unpatentable over Bhaskar in view of U.S. Patent No. 6,318,846 to Saul et al. (hereinafter, "Saul"). Applicant respectfully traverses the rejection.

The Examiner asserts Bhaskar for manufacturing a semiconductor device and then Saul for forming a plurality of FETs. However, as correctly asserted by the Office Action in relation to Claim 22, "Bhaskar et al. are silent as to the associated active areas 907 and 911 are formed after the exposing in

the first surface of the semiconductor substrate 901". *Office Action Dated March 31, 2004, Page 4.* Therefore, Bhaskar does not disclose, teach or suggest "forming first and second field effect transistors (FETs), wherein each said FET includes a gate electrode with associated active areas formed in the first surface of the semiconductor substrate having the current prevention layer thereon" as claimed in Claim 19. Saul does not cure the defects of Bhaskar. Accordingly, for at least this reason, this claim is allowable.

Claims 20-21 and **33** depend directly from claim 19 and are allowable for at least the same reasons as stated with respect to claim 19. These claims are also allowable for their own recited features which, in combination with those recited in claim 19, are neither shown nor suggested in the references of record, either singly or in combination with one another.

Claim 25 is rejected under 35 U.S.C. §103 as being unpatentable over Gardner in view of Liu. Applicant respectfully traverses the rejection. Claim 25 is a dependent claim which depends from claim 24 and therefore is allowable based on similar reasoning as described in relation to claim 24. Further, claim 25 is also allowable based on its own recited features which are not disclosed, taught, or suggested by Gardner nor Liu, alone or in combination.

The Examiner asserts that "Liu ... teach thermally growing a thermal oxide layer 32 before depositing the layer of oxide 36 on the first surface of the semiconductor substrate 25 (Figs 3A-3B)". *See Office Action Dated July 15, 2004.* To establish *prima facie* obviousness of a claimed invention, however, all the claim limitations must be taught or suggested by the prior art. *See In re Ryoka*, 180 U.S.P.Q. 580 (C.C.P.A. 1974). *See also In re Wilson*, 165 U.S.P.Q. 494 (C.C.P.A. 1970). As previously described, claim 24 recites "depositing a layer of oxide proximate a first surface of a semiconductor substrate",

"exposing a portion of the first surface of the semiconductor substrate", and "forming a pair of active areas in the exposed portion of the first surface, adjacent the deposited oxide layer". Claim 25 then recites "thermally growing a thermal oxide layer before depositing the layer of oxide on the first surface of the semiconductor substrate". Neither Gardner nor Liu, alone or in combination, disclose teach or suggest the "thermally growing", "depositing", "exposing" and "forming" as claimed. Accordingly, for at least this reason, claim 25 is allowable and withdrawal of the rejection is respectfully requested.

Conclusion

All pending claims 7-13 and 19-33 are in condition for allowance. Applicant respectfully requests reconsideration and prompt issuance of the subject application. If any issues remain that prevent issuance of this application, the Examiner is urged to contact the undersigned attorney before issuing a subsequent Action.

Respectfully submitted,

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By: _____

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